

What is claimed is:

1 1. A semiconductor device comprising:  
2 a semiconductor substrate in which a trench is formed;  
3 a liner layer formed of a multi-layer of a silicon nitride layer and a silicon oxide  
4 layer on the sidewalls and bottom of the trench by atomic layer deposition; and  
5 a buried insulating layer filled in the trench without a void.

1 2. The semiconductor device according to claim 1, further comprising:  
2 a plurality of gate stack patterns formed on the semiconductor substrate on  
3 which the trench and the buried insulating layer are formed;  
4 a plurality of gate spacers formed on the sidewalls of the gate stack patterns;  
5 a first bubble prevention layer formed of a multi-layer of a silicon oxide layer and  
6 a silicon nitride layer on the gate spacers by atomic layer deposition; and  
7 a first filling insulating layer filled without a void between the gate stack patterns  
8 on the first bubble prevention layer.

1 3. The semiconductor device according to claim 2, wherein the gate spacers  
2 are formed of a multi-layer of a silicon oxide layer and a silicon nitride layer by atomic  
3 layer deposition.

1 4. The semiconductor device according to claim 2, further comprising:  
2 a plurality of bit line stack patterns formed on the first filling insulating layer;  
3 a plurality of bit line spacers formed on the sidewalls of the bit line stack patterns;  
4 a second bubble prevention layer formed of a multi-layer of a silicon oxide layer  
5 and a silicon nitride layer on the bit line spacers and on the bit line stack patterns by  
6 atomic layer deposition; and  
7 a second filling insulating layer filled without a void between the bit line stack  
8 patterns on the second bubble prevention layer.

1 5. The semiconductor device according to claim 4, wherein the bit line  
2 spacers are formed of a multi-layer of a silicon oxide layer and a silicon nitride layer by  
3 atomic layer deposition.

1 6. The semiconductor device according to claim 1, wherein an oxide layer is  
2 formed by thermal oxidation or atomic layer deposition on the sidewalls and bottom of  
3 the trench before a liner layer is formed on the sidewalls and bottom of the trench.

1 7. The semiconductor device according to claim 2, wherein each gate stack  
2 pattern is formed by sequentially stacking a gate insulating layer, a first gate conductive  
3 layer, a second gate conductive layer, and a gate capping layer.

1 8. The semiconductor device according to claim 7, wherein the gate  
2 insulating layer is formed of a silicon oxide layer.

1 9. The semiconductor device according to claim 7, wherein the first gate  
2 conductive layer is formed of an impurity-doped polysilicon layer.

1 10. The semiconductor device according to claim 7, wherein the second gate  
2 conductive layer is formed of a metal silicide layer.

1 11. The semiconductor device according to claim 7, wherein the gate capping  
2 layer is formed of a silicon nitride layer.

1 12. The semiconductor device according to claim 4, wherein each bit line  
2 stack pattern is formed by sequentially stacking a barrier metal layer, a bit line  
3 conductive layer, and a bit line capping layer.

1 13. A semiconductor device comprising:  
2 a semiconductor substrate in which a trench is formed;  
3 a liner layer formed on the sidewalls and bottom of the trench;  
4 a buried insulating layer filled in the trench;

5 a plurality of gate stack patterns formed on the semiconductor substrate;  
6 a plurality of gate spacers formed on the sidewalls of the gate stack patterns;  
7 a first bubble prevention layer formed of a multi-layer of a silicon oxide layer and  
8 a silicon nitride layer on the gate spacers and on the patterned gate stacks by atomic  
9 layer deposition;  
10 a first filling insulating layer filled without a void between the gate stack patterns  
11 on the first bubble prevention layer;  
12 a plurality of bit line stack patterns formed on the first filling insulating layer;  
13 a plurality of bit line spacers formed on the sidewalls of the bit line stack patterns;  
14 a second bubble prevention layer formed of a multi-layer of a silicon oxide layer  
15 and a silicon nitride layer on the bit line spacers and the bit line stack patterns by atomic  
16 layer deposition; and  
17 a second filling insulating layer filled without a void between the bit line stack  
18 patterns on the second bubble prevention layer.

1 14. The semiconductor device according to claim 13, wherein the liner layer is  
2 formed of a multi-layer of a silicon nitride layer and a silicon oxide layer by atomic layer  
3 deposition, and the gate spacers and the bit line spacers are formed of a multi-layer of  
4 a silicon oxide layer and a silicon nitride layer by atomic layer deposition.

1 15. The semiconductor device according to claim 13, wherein an oxide layer is  
2 formed by thermal oxidation or atomic layer deposition on the sidewalls and bottom of  
3 the trench before a liner layer is formed on the sidewalls and bottom of the trench.

1 16. A method for fabricating a semiconductor device, the method comprising:  
2 forming a trench to a depth in a semiconductor substrate;  
3 forming a liner layer formed of a multi-layer of a silicon nitride layer and a silicon  
4 oxide layer on the sidewalls and bottom of the trench by atomic layer deposition; and  
5 forming a buried insulating layer filled in the trench without a void.

1 17. The method for fabricating a semiconductor device according to claim 16,  
2 wherein the liner layer is formed without a vacuum break.

1            18. The method for fabricating a semiconductor device according to claim 16,  
2 wherein the silicon nitride layer forming the liner layer is formed using silicon source of  
3 silane ( $\text{SiH}_4$ ), Si-alkyl, Si-halide, or Si-amide, and a nitrifying agent of ammonia, plasma  
4 ammonia, or plasma nitrogen.

1           19. The method for fabricating a semiconductor device according to claim 16,  
2 wherein the silicon oxide layer forming the liner layer is formed using silicon source of  
3 silane ( $\text{SiH}_4$ ), Si-alkoxide, Si-alkyl, Si-halide, or Si-amide, and an oxidizing agent of  
4 water ( $\text{H}_2\text{O}$ ), hydrogen peroxide, ozone, plasma  $\text{O}_2$ ,  $\text{N}_2\text{O}$ , or plasma  $\text{N}_2\text{O}$ .

20. The method for fabricating a semiconductor device according to claim 16,  
wherein an oxide layer is formed by thermal oxidation or atomic layer deposition on the  
sidewalls and bottom of the trench before a liner layer is formed on the sidewalls and  
bottom of the trench.

1            21.    The method for fabricating a semiconductor device according to claim 16,  
2    further comprising the steps of:

3        forming a plurality of gate stack patterns on the semiconductor substrate in which  
4        the trench and the buried insulating layer are formed;

5 forming a plurality of gate spacers on the sidewalls of the gate stack patterns;

6 forming a first bubble prevention layer of a multi-layer of a silicon oxide layer and

7 a silicon nitride layer on the gate spacers and the gate stack patterns by atomic layer  
8 deposition; and

9 forming a first filling insulating layer without a void between the gate stack  
10 patterns on the first bubble prevention layer.

22. The method for fabricating a semiconductor device according to claim 21,  
wherein the gate spacers are formed of a multi-layer of a silicon oxide layer and a  
silicon nitride layer by atomic layer deposition.

1            23.    The method for fabricating a semiconductor device according to claim 21,  
2    further comprising the steps of:

3 forming a plurality of bit line stack patterns on the first filling insulating layer;  
4 forming a plurality of bit line spacers on the sidewalls of the bit line stack  
5 patterns;  
6 forming a second bubble prevention layer of a multi-layer of a silicon oxide layer  
7 and a silicon nitride layer on the bit line spacers and the bit line stack patterns by atomic  
8 layer deposition; and  
9 forming a second filling insulating layer without a void between the bit line stack  
10 patterns on the second bubble prevention layer.

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2 24. The method for fabricating a semiconductor device according to claim 22,  
wherein the second bubble prevention layer is formed without a vacuum break.

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2 25. The method for fabricating a semiconductor device according to claim 22,  
wherein the bit line spacers are formed of a multi-layer of a silicon nitride layer and a  
3 silicon oxide layer by atomic layer deposition.

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2 26. The method for fabricating a semiconductor device according to claim 20,  
wherein each gate stack pattern is formed by sequentially stacking a gate insulating  
3 layer, a first gate conductive layer, a second gate conductive layer, and a gate capping  
4 layer.

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1 27. The method for fabricating a semiconductor device according to claim 26,  
2 wherein the gate insulating layer is formed of a silicon oxide layer.

1 28. The method for fabricating a semiconductor device according to claim 26,  
2 wherein the first gate conductive layer is formed of an impurity-doped polysilicon layer.

1 29. The method for fabricating a semiconductor device according to claim 26,  
2 wherein the second gate conductive layer is formed of a metal silicide layer.

1 30. The method for fabricating a semiconductor device according to claim 26,  
2 wherein the gate capping layer is formed of a silicon nitride layer.

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31. The method for fabricating a semiconductor device according to claim 22, wherein each bit line stack pattern is formed by sequentially stacking a barrier metal layer, a bit line conductive layer, and a bit line capping layer.

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32. A method for fabricating a semiconductor device, the method comprising the steps of:

forming a trench on a semiconductor substrate with a predetermined depth;  
forming a liner layer of a multi-layer of a silicon nitride layer and a silicon oxide layer on the sidewalls and bottom of the trench by atomic layer deposition;  
forming a buried insulating layer filled in the trench without a void;  
forming a plurality of gate stack patterns on the semiconductor substrate on which the trench and the buried insulating layer are formed;  
forming a plurality of gate spacers on the sidewalls of the gate stack patterns;  
forming a first bubble prevention layer of a multi-layer of a silicon oxide layer and a silicon nitride layer on the gate spacers and the gate stack patterns by atomic layer deposition;  
forming a first filling insulating layer without a void between the gate stack patterns on the first bubble prevention layer;  
forming a plurality of bit line stack patterns on the first filling insulating layer;  
forming a plurality of bit line spacers on the sidewalls of the bit line stack patterns;  
forming a second bubble prevention layer of a multi-layer of a silicon oxide layer and a silicon nitride layer on the bit line spacers and the bit line stack patterns by atomic layer deposition; and  
forming a second filling insulating layer without a void between the bit line stack patterns on the second bubble prevention layer.

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33. The method for fabricating a semiconductor device according to claim 32, wherein the liner layer is formed of a multi-layer of a silicon nitride layer and a silicon oxide layer by atomic layer deposition, and the gate spacers and the bit line spacers are formed of a multi-layer of a silicon oxide layer and a silicon nitride layer by atomic layer deposition.

1 34. The method for fabricating a semiconductor device according to claim 32,  
2 wherein the liner layer, the gate spacers, the first bubble prevention layer, the bit line  
3 spacers, or the second bubble prevention layer are formed without a vacuum break.

1 35. The method for fabricating a semiconductor device according to claim 32,  
2 wherein an oxide layer is formed by thermal oxidation or atomic layer deposition on the  
3 sidewalls and bottom of the trench before a liner layer is formed on the sidewalls and  
4 bottom of the trench.

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